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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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INTEL/BSTZ

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EXAMINER

SAVLA, ARPAN P

ART UNIT

PAPER NUMBER

2185

MAIL DATE

DELIVERY MODE

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PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/591,933	Applicant(s) SURESH ET AL.	
	Examiner Arpan P. Savla	Art Unit 2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 06 November 2009.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,5-8,12-15 and 19-21 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,5-8,12-15 and 19-21 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 06 November 2009 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Amendment

This Office action is in response to Applicant's communication filed November 6, 2009 in response to the Office action dated March 17, 2009. Claims 1, 5-8, 12-15, and 19-21 have been amended. Claims 2-4, 9-11, and 16-18 have been canceled. Claims 1, 5-8, 12-15, and 19-21 are pending in this application.

INFORMATION CONCERNING THE OATH/DECLARATION

Oath/Declaration

1. Applicant's oath/declaration filed November 6, 2009 has been reviewed by Examiner and is found to conform to the requirements prescribed in 37 CFR 1.63.

INFORMATION CONCERNING DRAWINGS

Drawings

2. Applicant's drawings submitted November 6, 2009 are accepted for examination.

ACKNOWLEDGMENT OF REFERENCES CITED BY APPLICANT

Information Disclosure Statement

3. As required by MPEP § 609(c), Applicant's submission of the Information Disclosure Statement (IDS) dated June 18, 2009 is acknowledged by the Examiner and the cited reference has been considered in the examination of the claims now pending.

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As required by MPEP § 609 c(2), a copy of the PTOL-1449 initialed and dated by the Examiner is attached to the instant Office action.

4. The IDS dated November 6, 2009 has not been considered because it is a duplicate of the IDS dated June 18, 2009 (which was considered).

OBJECTIONS

Claims

5. In view of Applicant's amendment, the objections to **claims 2-7 and 9-14** have been withdrawn.

REJECTIONS NOT BASED ON PRIOR ART

Claim Rejections - 35 USC § 101

6. In view of Applicant's amendment, the 101 rejection of **claims 15-21** has been withdrawn.

Claim Rejections - 35 USC § 112

7. In view of Applicant's amendment, the 112, second paragraph rejection of **claims 3, 4, 6, 7, 10, 11, 13, 14, 17, 18, 20, and 21** has been withdrawn.

REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

9. **Claims 1-21** are rejected under 35 U.S.C. 103(a) as being unpatentable over See et al. (U.S. Patent 6,226,728) (hereinafter "See") in view of Lasser (U.S. Patent Application Publication 2006/0253645).

10. **As per claims 1 and 15**, See discloses a method comprising:
writing data fragments to a non-volatile memory (col. 2, lines 11-21; col. 14, line 33; Fig. 18, element 1820); *It should be noted that the machine-readable storage device of claims 15 and 19-21 executes the same functions as the method of claims 1 and 5-7. Therefore, any reference(s) that teach claims 1 and 5-7 also teach the corresponding claims 15 and 19-21.*

updating entries of a sequence table to the non-volatile memory that identify locations of the data fragments written to the non-volatile memory (col. 14, lines 34-37; Fig. 18, element 1824; col. 5, lines 38-54; Figs. 5 and 6);

updating the sequence table when writing the data fragments to the non-volatile memory is completed (col. 14, lines 38-39 and 48-52; Fig. 18, element 1830; Fig. 19, elements 1910 and 1920).

See does not disclose that sequence table entries are stored in volatile memory;

and writing the sequence table from the volatile memory to the non-volatile memory at least one of when the sequence table is full and when writing the data fragments to the non-volatile memory is completed.

Lasser discloses a flash management table stored in volatile memory (paragraph 0059);

writing the sequence table from the volatile memory to the non-volatile memory when the sequence table is updated (paragraphs 0072 and 0082; Fig. 3, elements 214 and 230).

See and Lasser are analogous art because they are from the same field of endeavor, that being memory management systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to combine Lasser's fast wake-up of flash memory system with See's dynamic allocation of nonvolatile memory system, such that See's sequence table is stored on Lasser's RAM. In such a combination, when writing data fragments to non-volatile memory is completed, the sequence table is updated in RAM. In turn, when the sequence table is updated in RAM, the updated sequence table is written from RAM to the non-volatile memory. Therefore, such a combination discloses writing the sequence table from the volatile memory to the non-volatile memory at least one of when the sequence table is full and when writing the data fragments to the non-volatile memory is completed. The motivation for doing so would have been to achieve a fast wake-up time after powering it up even if the flash system software relies on management tables

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whose generation from scratch is time-consuming. This fast wake-up time is achieved without sacrificing data integrity.

11. **As per claims 5 and 19**, the combination of See/Lasser discloses updating a transaction indicator in the non-volatile memory prior to writing a transaction to the non-volatile memory (See, col. 14, lines 14-15 and 31-32; Fig. 17, element 1734; Fig. 18, element 1816);

and updating the transaction indicator in the non-volatile memory after writing the transaction to the non-volatile memory (See, col. 14, lines 54-56; Fig. 19, element 1940),

wherein the transaction comprises the data fragments and the sequence table (See, col. 14, lines 33-37; Fig. 18, elements 1820 and 1824).

12. **As per claims 6 and 20**, the combination of See/Lasser discloses allocating a data fragment header in the non-volatile memory prior to writing a data fragment of the data fragments to the non-volatile memory, wherein the data fragment header is associated to the data fragment (See, col. 14, lines 27-28; Fig. 18, element 1814);

and validating the data fragment header after writing the sequence table entries to the non-volatile memory (See, col. 14, lines 54-56; Fig. 19, element 1940).

13. **As per claims 7 and 21**, the combination of See/Lasser discloses allocating a sequence table header in the non-volatile memory prior to writing the sequence table to the non-volatile memory, wherein the sequence table header is associated with the sequence table (See, col. 14, lines 13-15; Fig. 17, element 1732);

and validating the sequence table header after writing the sequence table entries to the non-volatile memory (See, col. 14, lines 54-56; Fig. 19, element 1940).

14. **As per claim 8**, See discloses a system, comprising:

a non-volatile memory (col. 3, lines 21-22; Fig. 1, element 110);

a volatile memory (Fig. 1, element 130);

and a processor (Fig. 1, element 140) to:

write data fragments to a non-volatile memory (col. 2, lines 11-21; col. 14, line 33; Fig. 18, element 1820);

update entries of a sequence table to the non-volatile memory that identify locations of the data fragments written to the non-volatile memory (col. 14, lines 34-37; Fig. 18, element 1824; col. 5, lines 38-54; Figs. 5 and 6).

and update the sequence table when writing the data fragments to the non-volatile memory is completed (col. 14, lines 38-39 and 48-52; Fig. 18, element 1830; Fig. 19, elements 1910 and 1920).

See does not disclose that sequence table entries are stored in volatile memory; and writing the sequence table from the volatile memory to the non-volatile memory at least one of when the sequence table is full and when writing the data fragments to the non-volatile memory is completed.

Lasser discloses a flash management table stored in volatile memory (paragraph 0059);

writing the sequence table from the volatile memory to the non-volatile memory when the sequence table is updated (paragraphs 0072 and 0082; Fig. 3, elements 214 and 230).

See and Lasser are analogous art because they are from the same field of endeavor, that being memory management systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to combine Lasser's fast wake-up of flash memory system with See's dynamic allocation of nonvolatile memory system, such that See's sequence table is stored on Lasser's RAM. In such a combination, when writing data fragments to non-volatile memory is completed, the sequence table is updated in RAM. In turn, when the sequence table is updated in RAM, the updated sequence table is written from RAM to the non-volatile memory. Therefore, such a combination discloses writing the sequence table from the volatile memory to the non-volatile memory at least one of when the sequence table is full and when writing the data fragments to the non-volatile memory is completed. The motivation for doing so would have been to achieve a fast wake-up time after powering it up even if the flash system software relies on management tables whose generation from scratch is time-consuming. This fast wake-up time is achieved without sacrificing data integrity.

15. **As per claim 12**, the combination of See/Lasser discloses the processor further:

updates a transaction indicator in the non-volatile memory prior to writing a transaction to the non-volatile memory (See, col. 14, lines 14-15 and 31-32; Fig. 17, element 1734; Fig. 18, element 1816);

and updates the transaction indicator in the non-volatile memory after writing the transaction to the non-volatile memory (See, col. 14, lines 54-56; Fig. 19, element 1940),

wherein the transaction comprises the data fragments and the sequence table (See, col. 14, lines 33-37; Fig. 18, elements 1820 and 1824).

16. **As per claim 13**, the combination of See/Lasser discloses the processor further:

allocates a data fragment header in the non-volatile memory prior to writing a data fragment of the data fragments to the non-volatile memory, wherein the data fragment header is associated to the data fragment (See, col. 14, lines 27-28; Fig. 18, element 1814);

and validates the data fragment header after writing the sequence table entries to the non-volatile memory (See, col. 14, lines 54-56; Fig. 19, element 1940).

17. **As per claim 14**, the combination of See/Lasser discloses the processor further:

allocates a sequence table header in the non-volatile memory prior to writing the sequence table to the non-volatile memory, wherein the sequence table header is associated with the sequence table (See, col. 14, lines 13-15; Fig. 17, element 1732);

and validates the sequence table header after writing the sequence table entries to the non-volatile memory (See, col. 14, lines 54-56; Fig. 19, element 1940).

Response to Arguments

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18. Applicant's arguments filed November 6, 2009 with respect to **claims 1, 6-8, 13-15, 20, and 21** have been considered but are moot in view of the new ground(s) of rejection above.

19. Applicant's arguments filed November 6, 2009 with respect to **claims 5, 12, and 19** have been fully considered but they are not persuasive. In response to Applicant's argument that the references fail to show certain features of Applicant's invention, it is noted that the features upon which Applicant relies (i.e., "the transacted write...if a power loss happens after the transaction for writing the file is started, but before the transaction ends, parts of the file which have been written to the non-volatile memory may be deleted automatically by the power loss recovery feature") are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Accordingly, the combination of See/Lasser discloses the current language of claims 5, 12, and 19, as simply and broadly claimed by Applicant.

Conclusion

STATUS OF CLAIMS IN THE APPLICATION

The following is a summary of the treatment and status of all claims in the application as recommended by MPEP 707.70(i):

CLAIMS REJECTED IN THE APPLICATION

Per the instant office action, claims 1, 5-8, 12-15, and 19-21 have received an action on the merits and are subject of a final action.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Arpan P. Savla whose telephone number is (571) 272-1077. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah can be reached on (571) 272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Arpan Savla/
Examiner, Art Unit 2185
January 30, 2009

/Sanjiv Shah/
Supervisory Patent Examiner, Art
Unit 2185